REMARKS/ARGUMENTS

The title of the invention has been amended to more clearly describe the claimed subject matter. New claims 9 through 12 have also been added. No new matter has been added.

The Office Action mailed March 17, 2004, has been received and reviewed. Claims 1 through 8 are currently pending in the application. Claim 5 has been withdrawn from consideration as being drawn to a non-elected invention. Claims 1 through 4 and 6 through 8 stand rejected. Applicant has amended claims 1 and 2, and respectfully requests reconsideration of the application as amended herein.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,075,290 to Schaefer et al. in View of U.S. Patent No. 6,441,487 to Elenius et al.

Claims 1 through 4 and 6 through 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Schaefer et al.(U.S. Patent No. 6,075,290) in view of Elenius et al. (U.S. Patent No. 6,441,487). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 1 through 4 and 6 through 8 are improper because they fail to establish a *prima facie* case of obviousness.

Schaefer et al. is directed to chip scale packages having improved package interconnect structures for absorbing stresses introduced to bump type contacts on the chip scale packages

when attached to an external substrate. According to one disclosed embodiment, a chip scale package 200 comprises a die 202 having a conductive pad 204 formed thereon that may be coupled to at least one integrated circuit structure (Fig. 2 and col. 5, lines 21-28). A passivation layer 206 is formed on the surface of die 202 and forms a portion of a via 216 that is positioned over conductive pad 204. A resilient protective layer 208 is formed over portions of passivation layer 206 and also forms a portion of via 216 over conductive pad 204. An under bump pad 210 is formed within via 216 and over conductive pad 204. Alternatively, Schaefer et al. indicates that the via portion of protective layer 208 may be offset from the via portion of passivation layer 206, with conductive pad 204 being electrically coupled to under bump pad 210 by a redistribution layer (col. 5, lines 40-44). A contact bump 212 is formed over under bump pad 210 using conventional solder bumping or balling techniques for subsequent reflow to a board contact on an external substrate 214 (col. 6, lines 44-45 and col. 7, lines 8-13).

The Office indicates that Schaefer et al. does not show a conductive trace over a dielectric layer, but asserts it would be obvious to provide a conductive trace over a dielectric layer in view of the teachings of Elenius et al. Elenius et al. describes a chip scale package 8 comprising a semiconductor die formed from a wafer 14 having bond pads 18, 20 located proximate to an outer perimeter 21 of the semiconductor die (col. 6, lines 12-19). A passivation layer 22 is applied over the front surface of semiconductor wafer 14, and a first passivation layer 24 is optionally applied immediately above passivation layer 22 (Fig. 2 and col. 6, lines 20-36). Openings are formed in passivation layer 24 over bond pads 18, 20, and redistribution traces 30 formed over passivation layer 24 electrically connect bond pads 18, 20 to laterally displaced solder bump pads 26 (col. 6, lines 62-68). Elenius et al. indicates that this arrangement accomplishes a redistribution of the typical conductive bond pads to a new pattern, such as an array distribution pattern (col. 7, lines 29-32). A second passivation layer 32 is formed over redistribution traces 30, and solder balls 28 are formed upon and attached to solder pads 26 exposed through passivation layers 24 and 32 (col. 8, line 5-19).

Initially, Applicant submits that there is no suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art,

to modify the reference or combine reference teachings as suggested by the Office. The Office asserts that one of ordinary skill in the art would be motivated to provide the conductive trace disclosed by Schaefer et al. over a dielectric layer as taught by Elenius et al. "to provide an improved chip scale package ... not larger than the size of the original integrated circuit, and to internally redistribute the solder bump contact pads, away from the outer perimeter of the integrated circuit." However, Schaefer et al. already discloses that the described IC package embodiment is a wafer level chip scale package, and that chip scale packages have "overall package dimensions substantially equal to that of the silicon active device or die that is enclosed within the package" (col. 1, lines 46-50).

Likewise, Schaefer et al. does not disclose that conductive pads 204 are only located on the outside perimeter of die 202 and would require internal redistribution as suggested by the Office. Rather, Schaefer et al. states that "[t]he typical flip chip package includes an array of pads to provide interconnections" and that an "array configuration allows the engineer to utilize the package area for I/O pad placement, as opposed to other package designs, such as surface mount packages, which typically provide I/O pins only around the package periphery (col. 1, lines 37-45). Moreover, Schaefer et al. also discloses that the via portion of protective layer 208 may be offset from the via portion of passivation layer 206, with conductive pad 204 being electrically coupled to under bump pad 210 by a redistribution layer (col. 5, lines 40-44). As such, Schaefer et al. already discloses the features listed by the Office as being taught by Elenius et al., and there would, therefore, be no motivation to combine the references as presented.

Even if there were some motivation to combine Schaefer et al. and Elenius et al. as suggested by the Office, the resultant combination would fail to teach or suggest all the claim limitations. As amended herein, claim 1 recites the limitation of a metal-lined via, "wherein said metal-lined via is sized and configured to temporarily receive a substantially spherical interconnection element attached to a semiconductor device." Neither of Schaefer et al. or Elenius et al., alone or in combination, teach or suggest this limitation. Rather, Schaefer et al. discloses that contact bump 212 is formed over under bump pad 210 using conventional solder bumping or balling techniques for subsequent reflow to a board contact on an external substrate

214 (col. 6, lines 44-45 and col. 7, lines 8-13). Elenius et al. also teaches that a joint is formed between solder ball 28 and solder bump pad 26 (col. 8, lines 7-9).

In view of the foregoing, Applicant respectfully submits that claim 1 is allowable over the combination of Schaefer et al. and Elenius et al. under the provisions of 35 U.S.C. § 103(a). Claims 2 through 4 and 6 through 8, which depend from and incorporate all the limitations of claim 1, are also allowable. If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

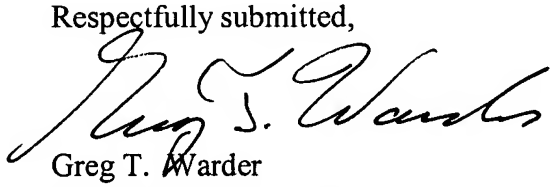
ENTRY OF AMENDMENTS AND NEW CLAIMS

The amendments to claims 1 and 2 above and new claims 9 through 12 should be entered by the Examiner because the amendments and new claims are supported by the as-filed specification and drawings and do not add any new matter to the application.

CONCLUSION

Claims 1 through 4 and 6 through 12 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Furthermore, claim 5, which is directed to a non-elected species, depends from claim 1. Applicant considers claim 1 to be generic and notes that upon allowance of a generic claim, all claims depending therefrom are also allowable. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,



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